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Helder, D.; Boucyk, W.; Morfitt, R.;

Geoscience and Remote Sensing Symposium Proceedings, 1998. IGARSS '98. IEEE International, Volume: 5, 6-10 July 1998

Pages:2716 - 2718 vol.5

[\[Abstract\]](#) [\[PDF Full-Text \(244 KB\)\]](#) **IEEE CNF**

2 Bandwidth-efficient trellis coded modulation schemes

Ramseier, S.;

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3 Coded modulation using superimposed binary codes

Xiao Ma; Li Ping;

Information Theory, IEEE Transactions on, Volume: 50, Issue: 12, Dec. 2000

Pages:3331 - 3343

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4 Multipurpose high-coding-gain 0.8- μ m BiCMOS VLSIs for high-speed multilevel trellis-coded modulation

Aikawa, S.; Nakamura, Y.; Takanashi, H.;

Solid-State Circuits, IEEE Journal of, Volume: 26, Issue: 11, Nov. 1991

Pages:1700 - 1707

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5 Combined iterative demapping and decoding for coded UWB-IR syst

Takizawa, K.; Kohno, R.;

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6 Predictive analog to digital conversion of Doppler ultrasound signals

Boe, S.; Kristoffersen, K.;

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8 Laser altimetry waveform measurement of vegetation canopy structure

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Aikawa, S.; Nakamura, Y.; Takanashi, H.;

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Min Zhao, Sachin S. Sapatnekar

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**

Full text available: [pdf \(114.02 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Domino logic is a high-performance circuit configuration that is usually embedded in static logic environment and tightly coupled with the clocking scheme. In this paper, the timing-driven partitioning algorithms that partition a logic network between (1) static and domino implementations, and (2) the phases of a two-phase clock, are provided. In addition, an efficient static mapping algorithm is described.

2 [Synthesis tools for mixed-signal ICs: progress on frontend and backend strategies](#)



L. Richard Carley, Georges G. E. Gielen, Rob A. Rutenbar, Willy M. C. Sansen

June 1996 **Proceedings of the 33rd annual conference on Design automation**

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3 [Special session on reconfigurable computing: Physical design methodologies for performance predictability and manufacturability](#)



Ricardo Reis, Fernanda Lima Kastensmidt, José Luís Güntzel

April 2004 **Proceedings of the first conference on computing frontiers on Computing frontiers**

Full text available: [pdf \(2.57 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The Physical Design Methodology of Integrated Systems is increasing its relevance in deep submicron technologies due to the appearance of new problems related to electrical behavior and performance predictability. This paper presents some techniques to improve reliability and manufacturability by the use of some layout strategies. One main approach is the search of regular solutions as the use of a layout composed by a matrix of cells. It is discussed the effects of layout strategies in the desi ...

Keywords: DFM, design methodologies, layout, physical design, regularity

4 [Group G: modeling and evaluation methodology: Constraint-guided dynamic](#)

reconfiguration in sensor networks

Sachin Kogekar, Sandeep Neema, Brandon Eames, Xenofon Koutsoukos, Akos Ledeczi, Miklos Maroti

April 2004 Proceedings of the third international symposium on Information processing in sensor networks

Full text available: [pdf \(388.61 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper presents an approach for dynamic software reconfiguration in sensor networks. Our approach utilizes explicit models of the design space of the embedded application. The design space is captured by formally modeling all the software components, their interfaces, and their composition. System requirements are expressed as formal constraints on QoS parameters that are measured at runtime. Reconfiguration is performed by transitioning from one point of the operation space to another based ...

Keywords: design space exploration, runtime/dynamic software reconfiguration

5 Special session on reconfigurable computing: Adaptive architectures for an OTN processor: reducing design costs through reconfigurability and multiprocessing

Tudor Murgan, Mihail Petrov, Mateusz Majer, Peter Zipf, Manfred Glesner, Ulrich Heinkel, Joerg Pleickhardt, Bernd Bleisteiner

April 2004 Proceedings of the first conference on computing frontiers on Computing frontiers

Full text available: [pdf \(1.01 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The standardisation process of Optical Transport Networks generally spans a long period of time. For providers intending to be present early on the market, this implies costly design re-spins if the wrong "flavour" of the protocol standard has been implemented. Extending a protocol processing device through application specific reconfigurable elements or multiprocessor units augment its flexibility. Thus, the architecture can be upgraded to standard updates or changes not even considered at desi ...

Keywords: ITU-T G.709, multiprocessor and reconfigurable architectures, optical transport networks, standard upgrades

6 Image transfer: an end-to-end design

Charles J. Turner, Larry L. Peterson

October 1992 ACM SIGCOMM Computer Communication Review , Conference proceedings on Communications architectures & protocols, Volume 22 Issue 4

Full text available: [pdf \(1.23 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The transfer of digital images between data archives and scientific workstations is likely to consume a significant amount of network bandwidth in the very near future. This paper examines the image transfer problem from an end-to-end perspective, that is, it describes a complete image transfer protocol that takes into account both the nature of digital imagery and the properties of the underlying network. Specifically, it describes a simple algorithm for encoding images into network packet ...

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